SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

FIELD

The disclosure relates to a structure, and more particularly to semiconductor structure and manufacturing method of the semiconductor.

BACKGROUND

Chip scale packages (CSP) are widely adopted for semiconductor chip assemblies in the industry because the component has a smaller size. A popular methodology of manufacturing a CSP component is a technology called surface mounting technology (SMT). The surface mounting technology is a method in which the semiconductor chip is mounted or placed directly on the surface of a printed circuit board (PCB). A semiconductor component made with SMT usually has either smaller bonding wires or no bonding wires at all.

Semiconductor chip enclosed in the chip scale component includes thousands of transistors and other miniaturized devices. The circuitry density keeps increasing as technology capability migrates from micron to nano scale. With a down-trending size, electronic products become more and more popular because its functionality and weight can fit in different occasions and applications.

However, heat generation in the packaged semiconductor component is discovered to be a drawback while people are celebrating the achievement of multi-chip stack package. Gaps in the three dimensional structure of a multi-chip stack are filled with materials like molding compound or other CTE match layer that traps heat inside the package. Undesired overheating is observed to be one of the major root causes of component malfunction. Some solutions such as adding fan or other external cooling to the component are implemented but still can not resolve the issue. Hence, a methodology to improve heat dissipation is still to be sought.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a cross sectional view of a semiconductor structure with dummy metal structure for dissipating heat in accordance with some embodiments of the present disclosure.

FIG. **2** is an enlarged view of the dummy metal structure and dummy bump in FIG. **1** including in accordance with some embodiments of the present disclosure.

FIG. **3** is a cross sectional view of a dummy metal structure and a dummy bump in contact with a heat sink in accordance with some embodiments of the present disclosure.

FIG. **4** is a cross sectional view of a dummy metal structure and a dummy bump in contact with a dummy heat conductive trace on a PCB in accordance with some embodiments of the present disclosure.

FIG. **5** is a flow chart diagram of a method for manufacturing a semiconductor structure in accordance with some embodiments of the present disclosure.

FIG. **6**A to FIG. **6**K are cross sectional views of a semiconductor structure at different operation stage in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION OF THE INVENTION

The manufacturing and use of the embodiments are discussed in details below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. It is to be understood that the following disclosure provides many different embodiments or examples for implementing different features of various embodiments. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting.

Further, it is understood that several processing steps and/or features of a device may be only briefly described. Also, additional processing steps and/or features can be added and certain of the following processing steps and/or features can be removed or changed while still implementing the claims. Thus, the following description should be understood to represent examples only, and are not intended to suggest that one or more steps or features is required.

In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

In the present disclosure, a heat dissipation structure is disposed on a semiconductor device to facilitate transferring thermal energy from the semiconductor device to ambient air. In some embodiments, the semiconductor device is in a chip-on-chip (COC) semiconductor structure, which is an integrated three dimensional stack of multiple semiconductor chips or dies. Heat generated inside the semiconductor device is dispelled by the heat dissipation structure disposed on a passive surface of the semiconductor device. The heat dissipation structure is fabricated to utilize some dummy conductive components without affecting device performance.

As used herein, "vapor deposition" refers to operations of depositing materials on a substrate using a vapor phase of a material to be deposited or a precursor of the material. Vapor deposition operations include any operations such as, but not limited to, chemical vapor deposition (CVD) and physical vapor deposition (PVD). Examples of vapor deposition methods include hot filament CVD, rf-CVD, laser CVD (LCVD), conformal diamond coating operations, metal-organic CVD (MOCVD), sputtering, thermal evaporation PVD, ionized metal PVD (IMPVD), electron beam PVD (EBPVD), reactive PVD, atomic layer deposition (ALD), plasma enhanced CVD (PECVD), high density plasma CVD (HDPCVD), low pressure CVD (LPCVD), and the like.

As uses herein, a "passive surface" refers to a surface of a semiconductor chip or die that is not configured to have any electrical terminal or contact for its normal operation. For example, for a semiconductor die, the passive surface is referred to a backside of the semiconductor die. Instead, an "active surface" is a surface including electrical terminal or contact for electrical connecting with an external circuit or device. In some embodiments, the active surface has metal pads exposing through a protective dielectric layer on top of the die. The metal pads are extension of internal circuitry of